Roll No. ..... **Total Pages : 02**

MT/D-21 49061

VLSI SIGNAL PROCESSING
MTECE-105N

Time : Three Hours] [Maximum Marks : 60

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. Explain the representation of DSP algorithms by using block diagram, signal flow graph and data flow graph by considering the system with output : **12**

$$y[n] = h_0x[n] + h_1x[n-1] + h_2x[n-2] + h_3x[n-3].$$

2. Describe any two iteration bound algorithms by taking an example. **12**

Unit II

3. (a) Explain Pipelining and Parallel processing for low power. **8**

(b) Consider a recursive filter $x(n) = ax(n-2) + u(n)$. Pipeline this multiply-add operator by 2 stages, by first breaking up the multiply-add operation into 2 components and by redistributing the delay elements in the loop. **4**

4. (a) Explain the properties of retiming. **8**

(b) Assuming $w_r(e_j) = w_{r,\max}$. Prove that $w_r(e_j) = w_{\max} + r(U) - r(U)$. **4**

Unit III

5. (a) Any feasible clock cycle period that can be obtained by retiming the J-unfolded DFG, G_i, can be achieved by retiming the original DFG, G, directly and then unfolding it by unfolding factor J. **6**

(b) Explain bit-level parallel processing. **6**

6. Explain Lifetime analysis and folding of multirate systems. **12**

Unit IV

7. Describe interleaved floorplan and bit plane based digital filters. **12**

8. Explain CORDIC algorithm in detail. **12**